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Experimental verification of single-phase PLL with novel two-phase generator for grid-connected converters

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Abstract — **For proper work of grid-connected converters it is important to have accurate detection of phase angle, frequency and amplitude of grid voltage. Estimation of these grid parameters can be achieved using PLL (phase locked loop) based on SRF (synchronous reference frame) theory. This PLL should have robustness against noise and offset introduced by measurement and data conversion. This paper proposes an improved PLL algorithm that has excellent noise and offset rejection property. The main part of proposed PLL is a novel two-phase generator which is used to obtain two quadrature signals for SRF block and PI regulator in closed control loop. Performances of proposed PLL are verified through experimental results given in this paper.**

Keywords — **PLL, two-phase generator, offset rejection.**

I. Introduction

In various grid-connected converters such as PWM rectifiers, uninterruptible power supply (UPS), distributed power systems, etc., it is very important to have information about phase angle, frequency and amplitude of grid voltage for their proper operation and control.

There is increasing interest for using PLL with different topologies for estimation of mentioned grid parameters [1]-[5]. In [3] is described PLL topology based on SRF for single-phase grid-connected converters. This topology requires the existence of two quadrature voltages (phase-shifted for $\pi/2$). In [3]-[6] is described a two-phase generator for obtaining these voltages using inverse Park's transformation. In [7] is proposed generating these signals using Hilbert transformer.

However, the main problem of these structures is the appearance of DC component (offset) in measured grid voltage. This DC component is usually caused by measurement and A/D conversion process. The offset causes errors in grid parameters estimation. In [4] it is shown that this error for single-phase grid voltage has the same fundamental harmonic component as grid voltage.

In order to eliminate this error, in [8]-[9] we proposed a novel two-phase generator which outputs two quadrature voltages and has the ability to eliminate grid offset. This generator is also robust against fast changes of grid parameters and successfully attenuates noise. It is adapted to grid frequency, so it can be used in all kinds of grid-connected converters.

In [8]-[9] we analyzed this novel PLL algorithm through simulations in Matlab/Simulink. In this paper experimental results of the same algorithm are given.

This paper is organized as follows: Section II describes the structure of proposed two-phase generator. Section III gives corresponding experimental results. The conclusion is given in section IV.

II. Novel Two-phase Generator With Offset Rejection

The general structure of proposed single-phase PLL, based on SRF theory, used in single-phase systems is shown in Fig. 1.

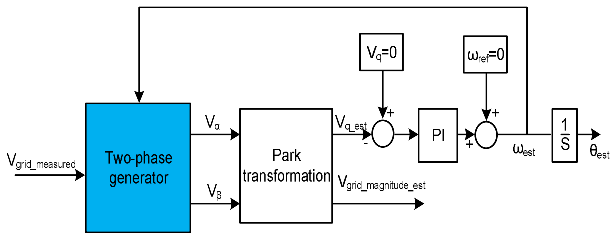

Fig. 1. The general structure of single-phase PLL based on SRF theory.

The key component of proposed PLL is two-phase generator which produces voltages v_α and v_β (phase-shifted for $\pi/2$) from input grid voltage v_{in}. Typically, it consists of second-order filters [5]. One of these two filters passes DC component of measured grid voltage, which causes estimation errors and makes estimation process impossible. This paper describes a new method of offset rejection which is based on closed control loop with simple integral action. The structure of novel two-phase generator is shown in Fig. 2 [9].

This structure consists of two parts: filters for obtaining voltages v_α and v_β (without outer control loop) and added feedback loop with integrator. Aim of added feedback loop is estimation of introduced DC offset. If we suppose that input grid voltage v_{in} contains DC offset, at the output of control loop estimated value of offset will be obtained and subtracted from input voltage.

From this structure two transfer functions can be derived:

$$W_{m\alpha}(s) = \frac{\omega s^2}{s^3 + (\omega + k_i)s^2 + \omega^2 s + k_i\omega^2} \quad (1)$$

$$W_{m\beta}(s) = \frac{\omega^2 s}{s^3 + (\omega + k_i)s^2 + \omega^2 s + k_i\omega^2}\,. \quad (2)$$

Both $W_{m\alpha}(s)$ and $W_{m\beta}(s)$ represent band-pass filters, which means that they don't pass DC component (offset) of input grid voltage, so they eliminate it.

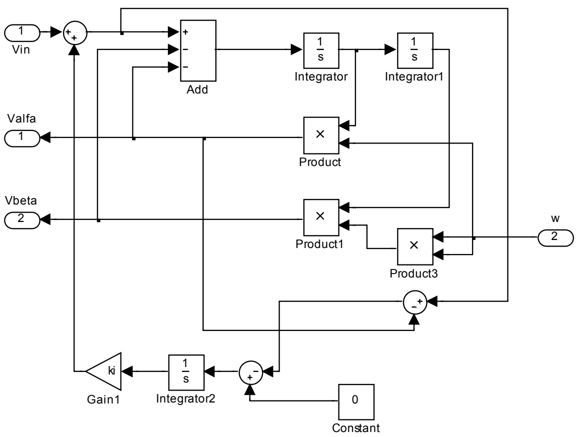

Fig. 2. The new two-phase generator with offset rejection realized in Matlab/Simulink environment.

The value of k_i determines the dynamics of the system's transient process. This value has main influence on speed of eliminating the estimation errors caused by grid offset.

III. Experimental Results of Proposed PLL

Performances of proposed two-phase generator as part of single-phase PLL were tested through experiments in Real-Time Windows Target environment of Matlab/Simulink. Block-diagram of proposed PLL topology, realized in Simulink, is shown in Fig. 3.

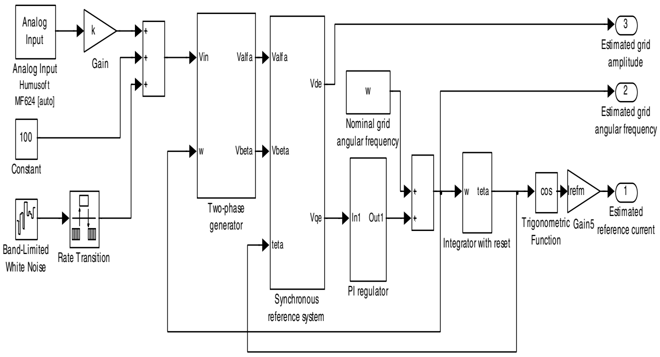

Fig. 3. Proposed PLL topology with novel two-phase generator.

Using Real-Time Windows Target makes the whole signal processing less difficult, because the algorithm from Fig. 3 isn't different from the one used in simulations [8]-[9]. The only difference is using block *Analog Input* as measured input grid voltage instead of *Sine Wave* source from Simulink library. This block is used as interface between real environment and control model in Simulink. The PCB interface was made for conditioning (galvanic isolate and scale) of grid voltage, which is then brought to A/D converter of HUMUSOFT MF 624 I/O card installed in PC. With *Analog Input* Simulink model of PLL gets the measured values of grid voltage from A/D converter.

With blocks *Constant* and *Band-Limited White Noise* (Fig. 3) offset and noise can be introduced into input grid voltage, simply adding their outputs to output of *Analog Input*.

Two forms of PLL were analyzed: continuous and discrete.

Grid voltage with $V_{RMS} = 230$V and frequency $f = 50$Hz was measured. The output from *Analog Input* block is in the range $(-10,10)$V. The gain k (Fig. 3) is the grid voltage scaling factor (transformer ratio, gain of interface PCB and A/D conversion gain).

A. Continuous Model of PLL

In continuous form, filters $W_{m\alpha}(s)$ and $W_{m\beta}(s)$ and other parts of PLL are realized in continuous time domain. This means that integrators in filter designs (Fig. 2) are realized in Laplace form 1/s.

In order to verify the influence of noise in measured grid voltage, Simulink block *Band-Limited White Noise* is added to input of two-phase generator. The experimental results for this case are shown in Fig. 4. Figure 4 shows waveforms of grid voltage v_{in} (with added noise), v_α and v_β. The height of the power spectral density (PSD) of white noise is 0.0095. It is obvious that two-phase generator successfully attenuates noise (filters $W_{m\alpha}(s)$ and $W_{m\beta}(s)$ are band-pass).

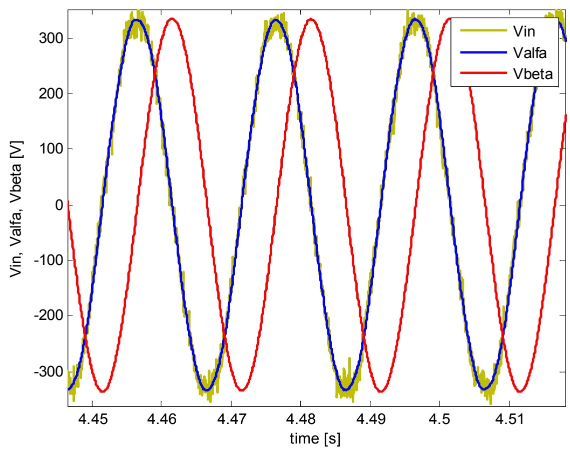

Fig. 4. The response of two-phase generator on grid voltage with noise.

Figures 5 and 6 show the results in case when offset is included in measured grid voltage (without noise), but without outer control loop for offset rejection. The value of offset is 100V (about 30%). There is a large ripple in estimated values of amplitude (Fig. 5) and frequency (Fig. 6) of grid voltage.

When control loop with integrator is included, the offset is successfully eliminated. This is shown in Fig. 7 and 8. The gain k_i is 100.

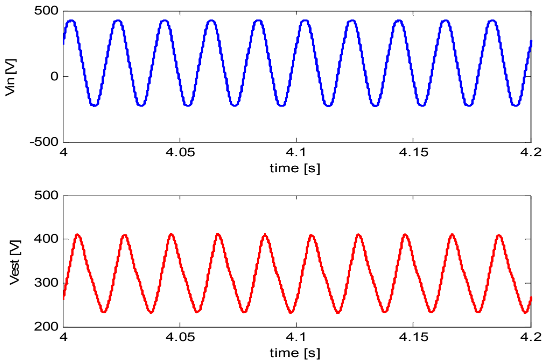

Fig. 5. Input grid voltage with 30% DC offset and estimated grid amplitude, without control loop.

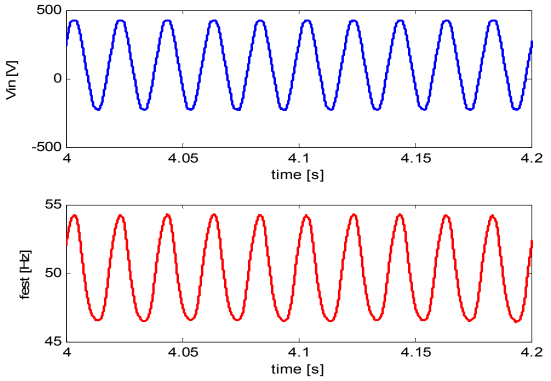

Fig. 6. Input grid voltage with 30% DC offset and estimated grid frequency, without control loop.

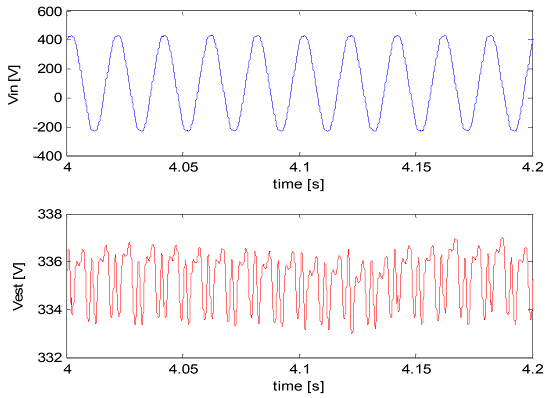

Fig. 7. Input grid voltage with 30% DC offset and estimated grid amplitude, with control loop.

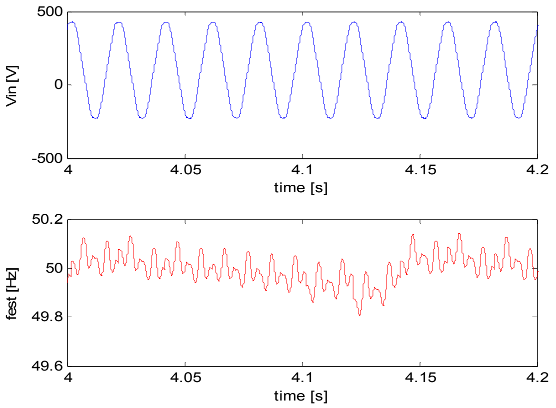

Fig. 8. Input grid voltage with 30% DC offset and estimated grid frequency, with control loop.

The ripple in estimated values, although it is very small, exists because the measured values of grid voltage differ from ideal sinusoid. There are several reasons for that: distortion of grid voltage, presence of quantization noise from A/D conversion process, fixed-step operation of Simulink model, etc.

It is important to verify robustness of whole system against fast changes of grid parameters. For this purpose two analog channels of MF 624 I/O card were used: one is for interface PCB and other is for function generator. Function generator outputs the sine wave with smaller amplitude then grid (PCB interface board) and lower frequency (47Hz). It contains 30% DC offset added in pure sine signal. At the time of 1s input of two-phase generator was switched from grid to function generator and vice versa at 2.5s.Three values of gain k_i were used (10, 100 and 500) to check its influence on dynamic behavior of whole system. The results are shown in Fig. 9. The response is fast and algorithm follows the frequency and amplitude changes very well.

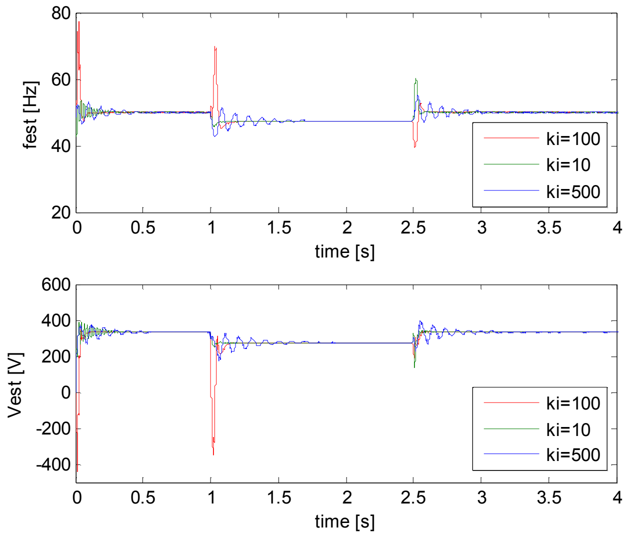

Fig. 9. Estimated grid frequency (top) and amplitude (bottom) for k_i = 10, 100 and 500.

One of the main tasks of PLL is to obtain the sinusoidal signal in phase with grid voltage which can be used as reference current for grid-connected inverter. Waveform of this signal together with input voltage is shown in Fig. 10.

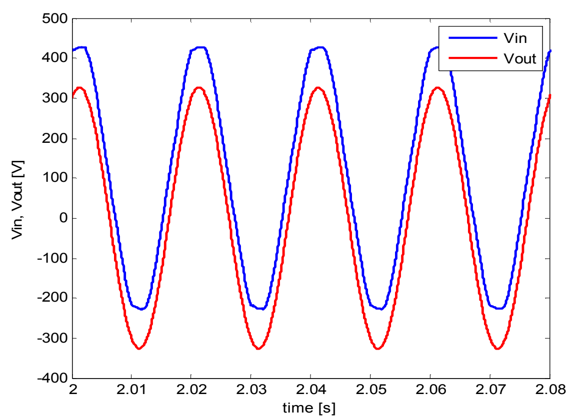

Fig. 10. Input grid voltage with 30% DC offset and generated reference voltage.

The results show that existence of 30% DC offset in measured grid voltage, in the case without control loop, causes appearance of about 10% second harmonic component in estimated refence current, which is unacceptable according to many standards.

B. Discrete Model of PLL

Lately, microprocessors and DSP such as dsPICs are widely used in signal processing. For this reason it was necessary to make a discrete form of proposed PLL.

It is very important to know how discretization process is performed and investigate if discretization process has influence on performances of proposed structure. There are many discrete time approximations, from low to high–order *s*-*z* transformation. Every form offers different characteristics in terms of dynamical behavior of applied process. With better discrete approximation of integrator $1/s$ the response of the process is better. In order to show the difference between different discretization forms, in this paper discretization was performed in two ways. The first one is based on Tustin approximation:

$$\frac{1}{s} \approx \frac{T_s}{2}\left(\frac{z+1}{z-1}\right). \qquad (3)$$

The other is based on Schneider approximation:

$$\frac{1}{s} \approx \frac{T_s}{12}\left(\frac{5+8z^{-1}-z^{-2}}{1-z^{-1}}\right). \qquad (4)$$

From Bode diagrams (Fig. 11) of discrete time integrators (3) and (4) is obvious that Tustin and Schneider approximations introduce different phase delays, which can affect transient response of the whole process.

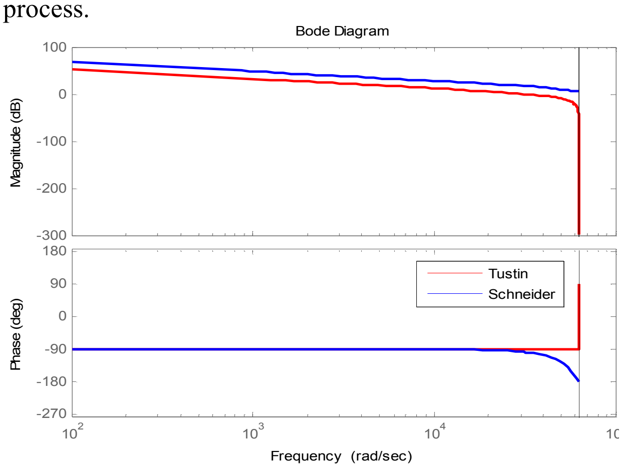

Fig. 11. Amplitude and phase characteristics of Tustin (red) and Schneider (blue) integrators.

Using approximations (3) and (4) two discrete models of PLL are obtained. The value of sample time T_s is 50μs and it is equal to fixed-step size of Simulink model solver. The value of sampling frequency has important influence on estimation process. It is recomended to have the value of sample time T_s as small as possible, because of grid period (about 20ms), speed and complexity of proposed PLL algorithm. With smaller sample time T_s we get more accurate estimation.

The results are very similar to those from continuous model. In Fig. 12 and 13 estimated values of grid amplitude and frequency are shown, respectively, for both discrete forms, in case of step changes of grid parameters. Grid frequency was changed from 50Hz to 47Hz, and amplitude was changed from $230V_{RMS}$ to $180V_{RMS}$. The value of gain k_i is 100. 30% DC offset was introduced to measured grid voltage.

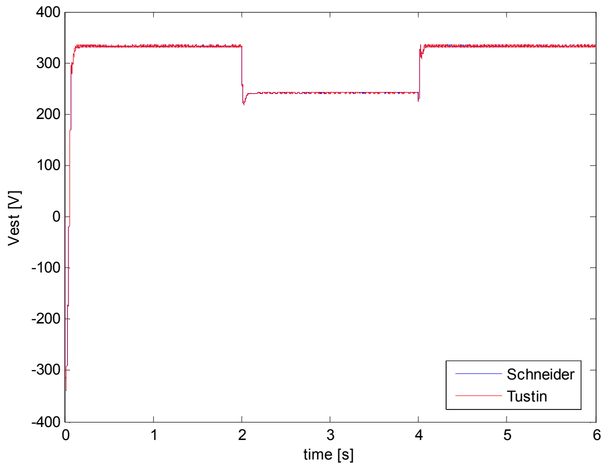

Fig. 12. Estimated grid amplitude for two discrete models of PLL

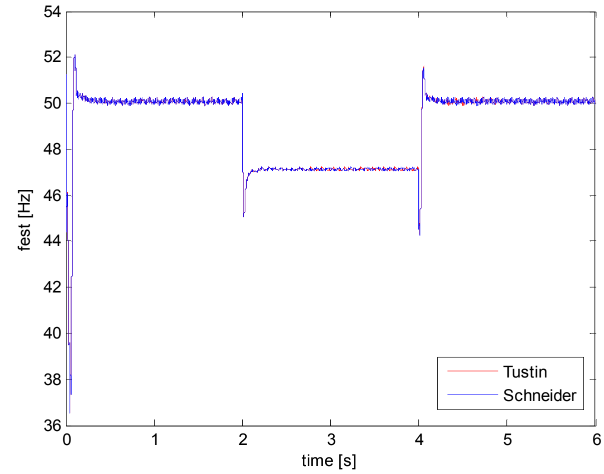

Fig. 13. Estimated grid frequency for two discrete models of PLL.

The results from Fig. 12 and Fig. 13 show that there is almost no difference between two discrete forms of PLL. In that case, using Tustin approximation, which is less order transformation than Schneider approximation, is quite satisfying.

IV. Conclusion

In this paper novel two-phase generator suitable for SRF PLL topology was analyzed and corresponding experimental results were given. The results show that proposed PLL (both continual and discrete) can solve important issues of presence of DC offset and noise in measured values of grid voltage. Therefore, proposed PLL can be used for both, grid-connected systems (e.g. Photovoltaic and Wind turbines) and power condition equipment (uninterruptible power supply (UPS), active filters) which rely on PLL based synchronization. The further work should be implementation of proposed PLL topology on digital platform (using dsPIC).

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